REMARKS

This application has been carefully reviewed in light of the Office Action dated April 5, 2004. Claims 19-24 remain in this application. Claims 19 and 22 are the independent Claims. Claims 19 and 22 have been amended. Support for the amendments are found, *inter alia*, on page 7, lines 7-11 and page 8, lines 9-14 in the specification. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Drawing Objection

The drawings were objected to under 37 CFR 1.83(a) for failing to show all the features of the invention.

In response, Applicant respectfully points out that Figs. 5 and 6 show a substrate 52 or another IC chip which is integrated with an IC chip 51. Similarly, page 8, line 20 of the specification reads "a substrate 52 (or another IC chip)". Moreover, page 10, line 19 of the specification reads "with the substrate 52 or with another IC chip". These descriptions clearly show that "a substrate 52" and "another IC chip" are equal (equivalent). As a consequence, the mark "52" shown in Figs. 5 and 6 illustrate both "a substrate 52" and "another IC chip".

Reconsideration and withdrawal of the above objections are respectfully requested.

Claim Objection

Claim 22 was objected to because of an informality. In response, Applicant has amended that claim to address the concern of the above objection. Reconsideration and withdrawal of the above objection are respectfully requested.

Art-Based Rejections

Claims 19-24 were rejected under 35 U.S.C. 103(a) over U.S. Patent No. 6,278,128 (Noji) in view of Japanese Patent No. 63-122150 (Yamaguchi). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Noji Reference

Noji is directed to wire bonding pads serving as circuit terminals that are arranged near the center of a chip on which a semiconductor circuit is formed. *(See Noji; Col. 9, lines 27-29).* An organic substrate and a wiring pattern are formed on the chip, wherein the wiring pattern has bonding regions for bonding wires near the wire bonding pads, and wherein fuses can be interposed between the wire bonding pads. *(See, Noji; Col. 9, lines 29-36; Col. 10, lines 55-57).*

The Yamaguchi Reference

The ancillary Yamaguchi reference is directed to a fuse having two parts where the fuse can be cut. *(See, Yamaguchi; Page 1, lines 11-12).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a chip having externally and selectively cuttable members.

Claim 19

As defined by amended independent Claim 19, an IC chip includes at least one externally and selectively cuttable member having at least one cuttable section. The cuttable member includes a multiplicity of cuttable points. The cuttable member remains cut open so long as at least one cuttable point remains cut open.

The cuttable member includes a multiplicity of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with a logic circuit, which function as if said cuttable sections were physically connected in series.

The applied references of record do not disclose or suggest the above features of the present invention as defined by amended independent Claim 19. In particular, neither Noji nor Yamaguchi disclose or suggest, "said cuttable member includes a multiplicity of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with a logic circuit, which function as if said cuttable sections were physically connected in series," as required by amended independent Claim 19.

The present invention discloses a chip having externally and selectively cuttable members. In one aspect, the cuttable members can be formed in the chip so that the characteristics of the elements, such as resistances and capacitances, involved in the IC chip can be adjusted, or so that logical states of logical circuits can be determined by selectively cutting some of the cuttable members. *(See, e.g. Application; Fig. 1; Page 5, lines 1-5).*

In contrast, the applied Noji reference is directed to wire bonding pads serving as circuit terminals that are arranged near the center of a chip on which a semiconductor circuit is formed. *(See, Noji; Col. 9, lines 27-29).* In Fig. 6A, Noji illustrates cuttable members. However, these cuttable members are interposed between wire bonding pads in a parallel arrangement. Clearly, as illustrated in Fig. 6A, Noji does not teach or suggest the use of "said cuttable member includes a multiplicity of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with a logic circuit, which function as if said cuttable sections were physically connected in series," as required by amended independent Claim 19. Moreover, as shown in Fig. 9, the logic

circuits disclosed by Noji receive signals from fuses. However, the composition of those fuses and of those logic circuits and the effect obtained by the result are all clearly different from those of this invention. Moreover, the Noji does not disclose or suggest "cuttable member remains cut open so long as at least one cuttable point remains cut open," as required by amended independent Claim 19.

Accordingly, Noji does not disclose or suggest the above features of the present invention.

The ancillary Yamaguchi reference does not remedy the above deficiencies of Noji.

Since the applied references fail to disclose, teach or suggest the above features recited in amended independent Claim 19, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of those claims.

Accordingly, independent Claim 19 is believed to be in condition for allowance and such allowance is respectfully requested.

Claim 22

As defined by amended independent Claim 22, a semiconductor device includes an IC chip having at least one externally and selectively cuttable member including at least one cuttable section. The cuttable member includes a multiplicity of cuttable points. The cuttable member working normally when at least one of the cuttable points remains cut open. The cuttable member also includes bumps formed on the same side of the IC chip as the cut member in association with respective cuttable points. A substrate or another IC chip. A connection member made of an anisotropic conductor and sandwiched between said IC chip and said substrate or another IC chip. The IC chip and the substrate or another IC chip are pressed together. The cuttable member includes a multiplicity

of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with a logic circuit, which function as if said cuttable sections were physically connected in series.

The Applicant respectfully submits that amended independent Claim 22 is allowable for at least the reasons discussed in connection with amended independent Claim 19.

Moreover, Applicant respectfully submits that Yamaguchi does not disclose or suggest "connection member made of an anisotropic conductor, " as required by amended independent Claim 22. Since Yamaguchi does not disclose or suggest connecting an IC chip and a substrate (or another IC chip), it can be fairly concluded that "a connection member made of an anisotropic conductor" is not disclosed by Yamaguchi.

Moreover, neither Noji nor Yamaguchi disclose or suggest using "an anisotropic conductor" as a connection member where "an anisotropic conductor" is not used.

Since the applied references fail to disclose, teach or suggest the above features recited in independent Claim 22, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of those claims.

Accordingly, independent Claim 22 is believed to be in condition for allowance and such allowance is respectfully requested.

The remaining rejected claims depend either directly or indirectly from independent Claims 19 and 22 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

Conclusion

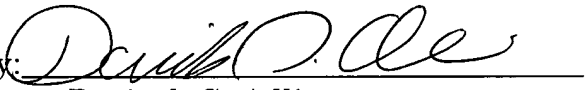
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: July 2, 2004

By: 

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